DERWENT-ACC-NO: 2002-477652

DERWENT-WEEK: 200251

TITLE: Method for manufacturing flash memory cell

INVENTOR: JUNG, S M; KIM, J S ; LEE, S B

PATENT-ASSIGNEE: HYNIX SEMICONDUCTOR INC[HYNIN]

PRIORITY-DATA: 2000KR-0035681 (June 27, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2002001247 A	January 9, 2002	N/A	001	H01L 021/8247

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2002001247A	N/A	2000KR-0035681	June 27, 2000

INT-CL (IPC): H01L021/8247

ABSTRACTED-PUB-NO: KR2002001247A

BASIC-ABSTRACT:

NOVELTY - A method for manufacturing a flash memory cell is provided to reduce a cell size and to prevent a control gate from being in direct contact with a semiconductor substrate, by forming a gap between floating gates smaller than a minimum design rule.

DETAILED DESCRIPTION - An isolation layer(22) is formed in a predetermined region of the semiconductor substrate(21). A tunnel oxide layer(23), the first polysilicon layer(24), an oxide layer and a nitride layer are sequentially formed on the resultant structure. The nitride layer and the oxide layer are patterned to expose a predetermined region of the first polysilicon layer. An insulation layer is formed on the resultant structure, and is blank-etched to form a spacer(25) on the sidewall of the stacked structure of the pattern oxide layer and nitride layer. The first polysilicon layer and the tunnel oxide layer are patterned by an etch process using the oxide layer and nitride layer patterns as a mask. After the spacer, the nitride layer and the oxide layer are eliminated, a dielectric layer(26) and the second polysilicon layer(27) are formed on the resultant structure, and are patterned to form the control gate.

CHOSEN-DRAWING: Dwg.1/10

DERWENT-CLASS: L03 U11 U12

CPI-CODES: L03-G04A; L04-C06; L04-C10B; L04-C12A; L04-C12B;

EPI-CODES: U11-C18B5; U12-D02A1;

Basic Abstract Text - ABTX (2):

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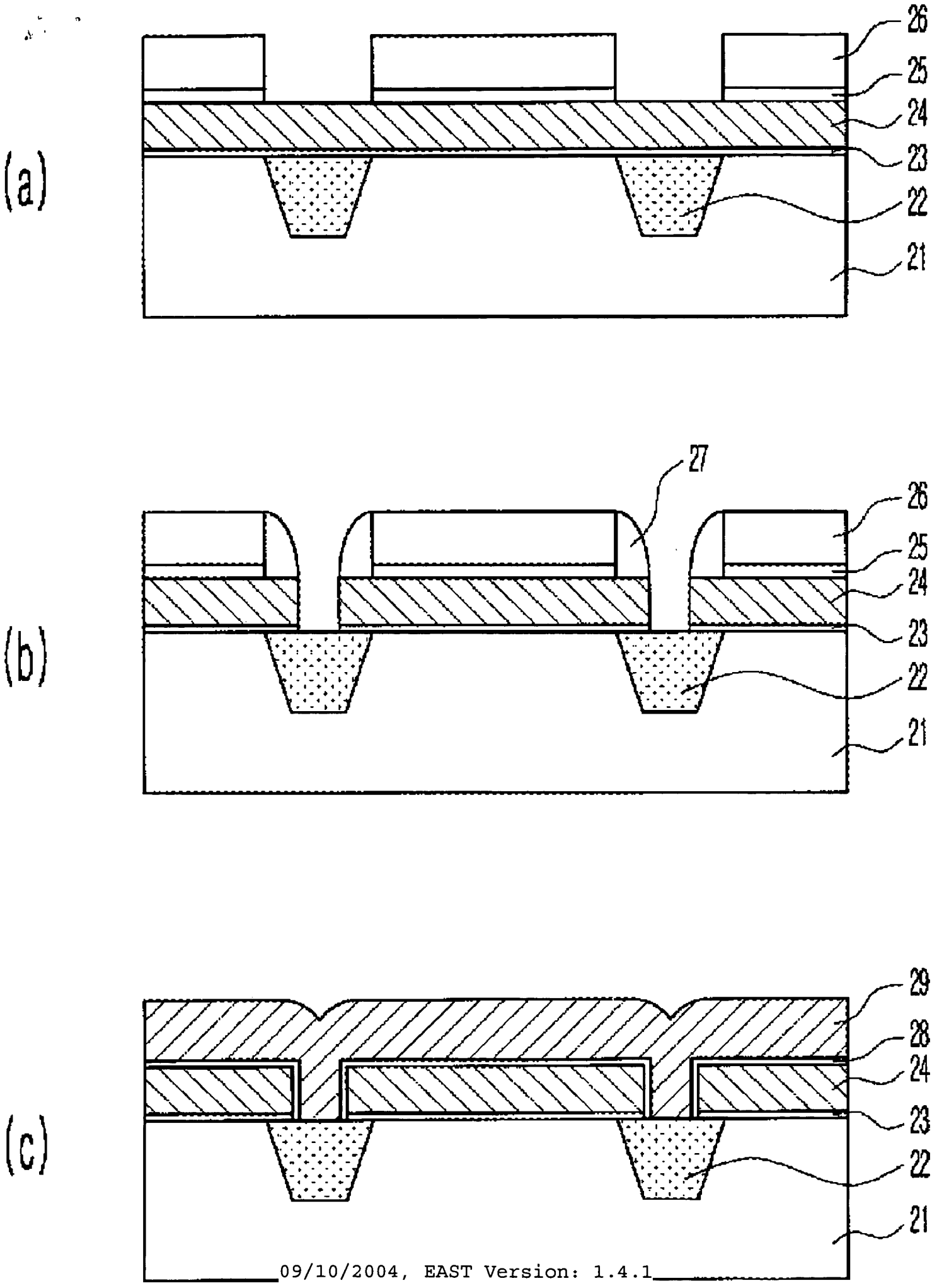
Derwent Accession Number - NRAN (1):

2002-477652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